REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

Disposition of Claims

Claims 1-12, 15, 17, and 18 are pending in the present application. Claims 1 and 13 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 13.

Claim Amendments

Independent claims 1 and 13 have been amended to clarify the present invention. No new matter has been added by way of these amendments, as support for these amendments may be found, for example, in Figure 5 of the Specification. Additionally, claims 8 and 18 were amended solely for proper antecedent basis reasons.

Rejection(s) under 35 U.S.C § 102

Claims 1-3, 5-13, 15, 17, and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,150,861 issued to Matsunaga *et al.* (hereinafter "Matsunaga"). Claims 1 and 13 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to a flip-flop circuit with embedded scan capabilities. With reference to the exemplary embodiment shown in Figure 5 of the present application, a flip-flop **80** includes a scan input control stage **127** that is connected to a scan node **SN** and a data input control stage **123** that is connected to a data node **DN**, where the data node

DN and the scan node **SN** each connect to a master stage **82** of the flip-flop **80**. The master stage **82** is also connected to a slave stage **84** of the flip-flop **80**.

With further reference to the exemplary embodiment shown in Figure 5 of the present application, a clock input control stage **99** generates a plurality of clock signals dependent on the clock input CLK and inverters **98, 100, 102, 104**. The plurality of clock signals generated by the clock input control stage **99** are used to control the master stage **82**, the slave stage **84**, the data input control stage **123**, and the scan input control stage **127**. For example, the outputs of inverters **98** and **104** are used to control the states of the data input control stage **123** and scan input control stage **127**. Further, the output of inverter **104** is used to control the master stage **82** and the slave stage **84**. Accordingly, the plurality of clock signals generated by the clock input control stage **99** are used to control the master stage **82**, the slave stage **84**, the data input control stage **123**, and the scan input control stage **127**.

Accordingly, amended independent claims 1 and 13 require, in part, that a plurality of clock signals are used to control the data input control stage, the scan input control stage, the master stage, and the slave stage.

Matsunaga, in contrast to the present invention, fails to disclose at least the limitations of independent claims 1 and 13 discussed above. Matsunaga is directed to a flip-flop that eliminates line delays between the flip-flops of a shift register (*see* Matsunaga, col. 1, lines 35-37; col. 2, lines 1-7). Matsunaga discloses that the CLK(II) signal is significantly delayed relative to the CLK(I) signal *due to delays in the clock line* (*see* Matsunaga col. 3, lines 40-44). As shown in Figure 1 of Matsunaga, a clock signal is input from a clock **18** to flip-flops **12, 14,** and **16**. Figure 2 of Matsunaga shows a representative flip-flop **12**. As clearly shown in Figure 2 of Matsunaga, the same phase of the clock signal CLK is used to control the purported master stage **36**, the purported slave stage **48**, and the purported latch **22**. Accordingly, it is clear in

Matsunaga that a plurality of control signals are not generated in the flip-flop. Thus, Matsunaga necessarily cannot disclose a plurality of clock signals that are used to control the data input control stage, the scan input control stage, the master stage, and the slave stage, as required by amended independent claims 1 and 13 of the present application. The delay inherent in a signal line among a plurality of flip-flops is not equivalent to a clock signal generated by a clock input control stage internally in an individual flip-flop. Matsunaga is completely silent as to generating a plurality of clock signals to control portions of flip-flop **12, 14,** or **16**.

Further, as shown in Figure 2 of Matsunaga, the purported master flip-flop **36,** purported slave flip-flop **48,** and purported latch **22** are each controlled by the same phase of the clock signal **CLK**. Scan data **SD** or signal data **D** is selected by scan enable signal **SCAN** at multiplexer **34.** The clock signal **CLK** is not used to control any value outputted from multiplexer **34**. Thus, the purported scan input stage **22** is not controlled by *any* clock signal generated by a clock input control stage.

In view of the above, Matsunaga fails to show or suggest the present invention as recited in amended independent claims 1 and 13. Thus, amended independent claims 1 and 13 are patentable over Matsunaga. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/082001).

Dated: February 3, 2005

Respectfully submitted,

By _____

Wasif H. Qureshi
Registration No.: 51,048
Osha & May L.L.P.
1221 McKinney, Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)

83249_1.DOC

Application No. (if known): 09/822,166 Attorney Docket No.: 03226/082001; P5751

Certificate of Express Mailing Under 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. EV562274860US in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on February 3, 2005
Date

Signature

Yuki Tsukuda
Typed or printed name of person signing Certificate

Registration Number, if applicable

(713) 228-8600
Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.